CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08

1.8V 4k/8k/16k x 16 and 8k/16k x 8 ConsuMoBL Dual-Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- 4/8/16k × 16 and 8/16k × 8 organization
- High-speed access: 40 ns
- Ultra Low operating power
  - — Active: I_{CC} = 15 mA (typical) at 55 ns
  - — Active: I_{CC} = 25 mA (typical) at 40 ns
  - — Standby: I_{SB3} = 2 µA (typical)
- Port-independent 1.8V, 2.5V, and 3.0V I/Os
- Lead (Pb)-free 14 x 14 x 1.4 mm 100-pin TQFP Package
- Full asynchronous operation
- Pin select for Master or Slave
- Expandable data bus to 32 bits with Master/Slave chip select when using more than one device
- On-chip arbitration logic
- On-chip semaphore logic
- Input Read Registers and Output Drive Registers
- $\overline{\text{INT}}$ flag for port-to-port communication
- Separate upper-byte and lower-byte control
- Commercial and industrial temperature ranges

Selection Guide for V_{CC} = 1.8V

	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55	Unit
Port I/O Voltages (P1-P2)	**1.8V-1.8V**	**1.8V-1.8V**	
Maximum Access Time	40	55	ns
Typical Operating Current	25	15	mA
Typical Standby Current for I_{SB1}	2	2	µA
Typical Standby Current for I_{SB3}	2	2	µA

Selection Guide for V_{CC} = 2.5V

	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55	Unit
Port I/O Voltages (P1-P2)	**2.5V-2.5V**	**2.5V-2.5V**	
Maximum Access Time	40	55	ns
Typical Operating Current	39	28	mA
Typical Standby Current for I_{SB1}	6	6	µA
Typical Standby Current for I_{SB3}	4	4	µA

Selection Guide for V_{CC} = 3.0V

	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55	Unit
Port I/O Voltages (P1-P2)	**3.0V-3.0V**	**3.0V-3.0V**	
Maximum Access Time	40	55	ns
Typical Operating Current	49	42	mA
Typical Standby Current for I_{SB1}	7	7	µA
Typical Standby Current for I_{SB3}	6	6	µA

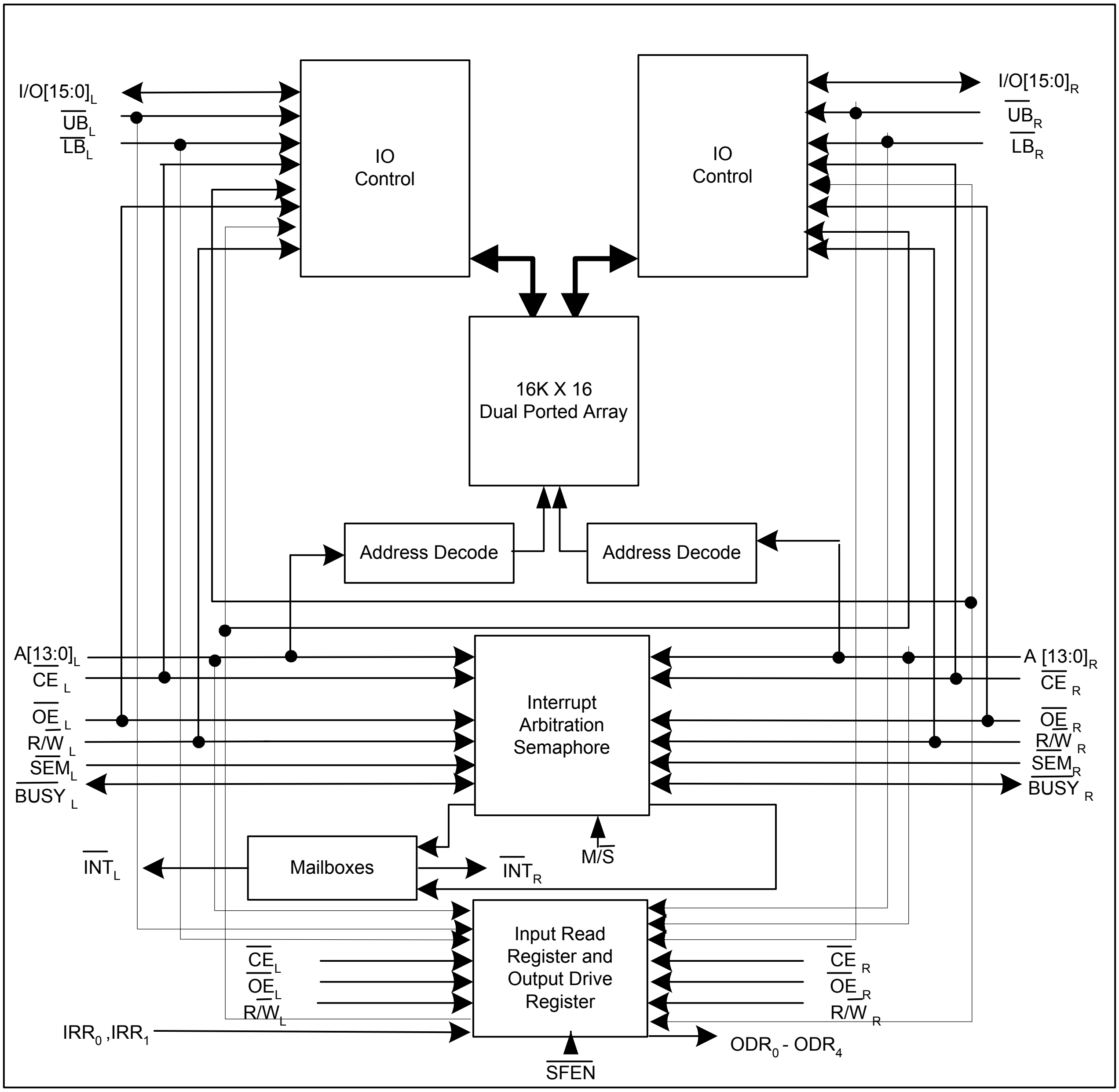
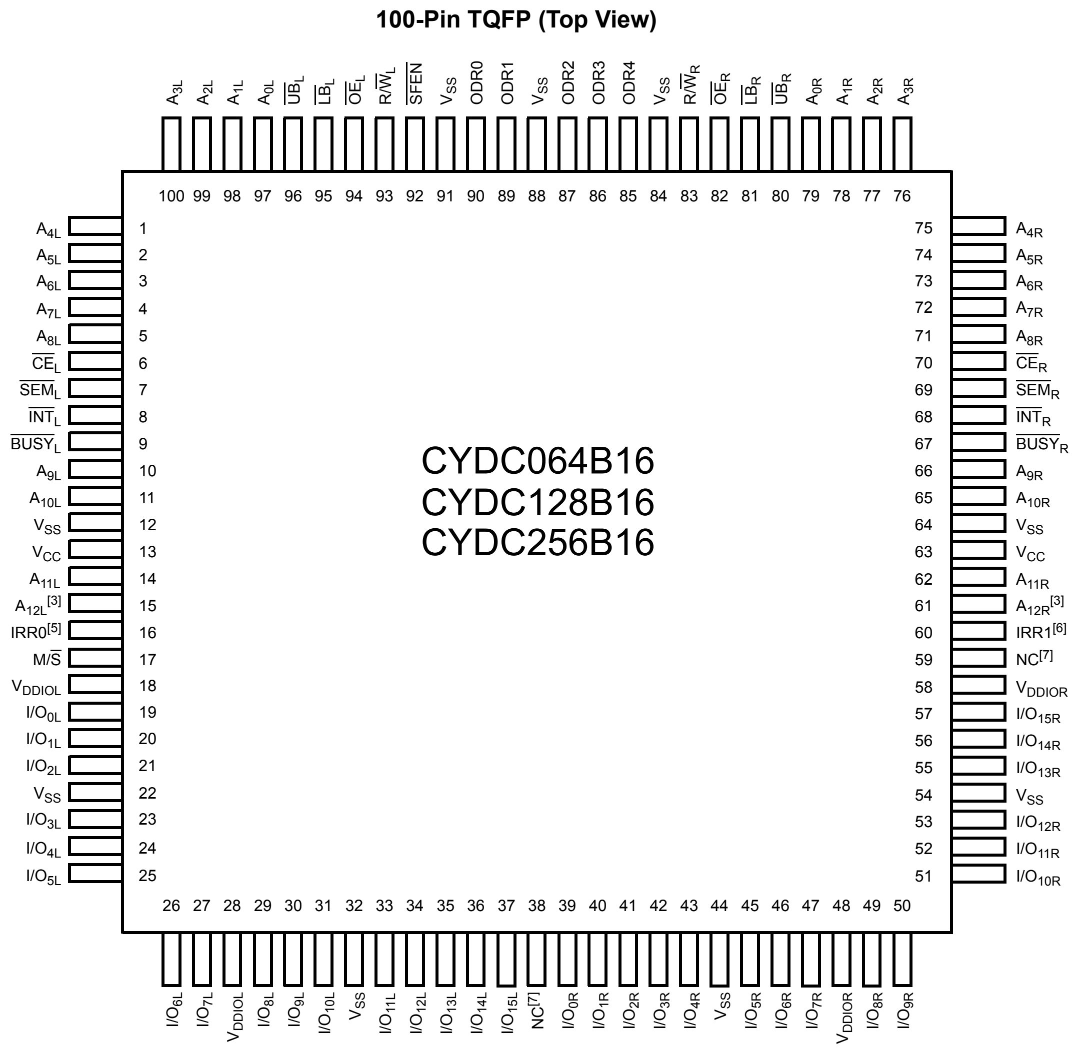


Figure 1. Top Level Block Diagram[1, 2]

Notes:
1. A_0–A_{11} for 4k devices; A_0–A_{12} for 8k devices; A_0–A_{13} for 16k devices.
2. BUSY is an output in master mode and an input in slave mode.

Pin Configurations [3, 4, 5, 6, 7]

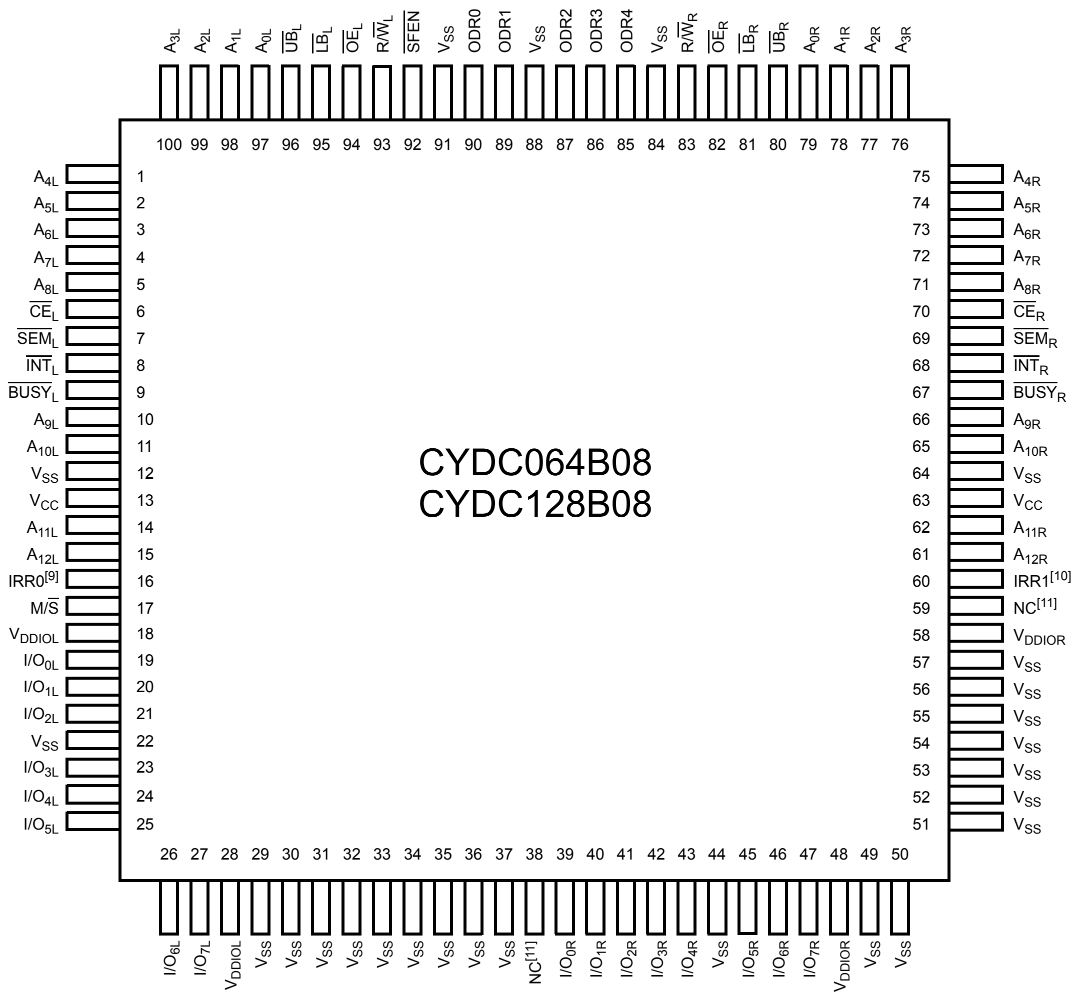


Notes:

3. A12L and A12R are NC pins for CYDC064B16.
4. IRR functionality is not supported for the CYDC256B16 device.
5. This pin is A13L for CYDC256B16 device.
6. This pin is A13R for CYDC256B16 device.
7. Leave this pin unconnected. No trace or power component can be connected to this pin.

Pin Configurations (continued)[7, 8, 9, 10]

100-pin TQFP (Top View)



Notes:

8. IRR functionality is not supported for the CYDC128B08 device.
9. This pin is A13L for CYDC128B08 devices.
10. This pin is A13R for CYDC128B08 devices.

Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	**Chip Enable**
$R/\overline{W}_L$	$R/\overline{W}_R$	**Read/Write Enable**
$\overline{OE}_L$	$\overline{OE}_R$	**Output Enable**
$A_{0L}–A_{13L}$	$A_{0R}–A_{13R}$	**Address ($A_0–A_{11}$ for 4k devices; $A_0–A_{12}$ for 8k devices; $A_0–A_{13}$ for 16k devices)**.
$I/O_{0L}–I/O_{15L}$	$I/O_{0R}–I/O_{15R}$	**Data Bus Input/Output for x16 devices; $I/O_0–I/O_7$ for x8 devices.**
$\overline{SEM}_L$	$\overline{SEM}_R$	**Semaphore Enable**
$\overline{UB}_L$	$\overline{UB}_R$	**Upper Byte Select ($I/O_8–I/O_{15}$ for x16 devices; Not applicable for x8 devices)**.
$\overline{LB}_L$	$\overline{LB}_R$	**Lower Byte Select ($I/O_0–I/O_7$ for x16 devices; Not applicable for x8 devices)**.
$\overline{INT}_L$	$\overline{INT}_R$	**Interrupt Flag**
$\overline{BUSY}_L$	$\overline{BUSY}_R$	**Busy Flag**
IRR0, IRR1		**Input Read Register for CYDC064B16, CYDC064B08, CYDC128B16. A13L, A13R for CYDC256B16 and CYDC128B08 devices.**
ODR0-ODR4		**Output Drive Register; These outputs are Open Drain.**
$\overline{SFEN}$		**Special Function Enable**
$M/\overline{S}$		**Master or Slave Select**
V_{CC}		**Core Power**
GND		**Ground**
V_{DDIOL}		**Left Port I/O Voltage**
V_{DDIOR}		**Right Port I/O Voltage**
NC		**No Connect**. **Leave this pin Unconnected.**

Functional Description

The CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 are low-power CMOS 4k, 8k,16k x 16, and 8/16k x 8 dual-port static RAMs. Arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 16-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 32-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable ($R/\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a Chip Enable ($\overline{CE}$) pin.

The CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 are available in 100-pin TQFP packages.

Power Supply

The core voltage (V_{CC}) can be 1.8V, 2.5V or 3.0V, as long as it is lower than or equal to the I/O voltage.

Each port can operate on independent I/O voltages. This is determined by what is connected to the V_{DDIOL} and V_{DDIOR} pins. The supported I/O standards are 1.8V/2.5V LVCMOS and 3.0V LVTTL.

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of $R/\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $R/\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}$ pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag,

then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CYDC064B16, 1FFF for the CYDC128B16 and CYDC064B08, 3FFF for the CYDC256B16 and CYDC128B08) is the mailbox for the right port and the second-highest memory location (FFE for the CYDC064B16, 1FFE for the CYDC128B16 and CYDC064B08, 3FFE for the CYDC256B16 and CYDC128B08) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user-defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin. On power up, an initialization program should be run and the interrupts for both ports must be read to reset them.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2.*

Busy

The CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Input Read Register

The Input Read Register (IRR) captures the status of two external input devices that are connected to the Input Read pins.

The contents of the IRR read from address x0000 from either port. During reads from the IRR, DQ0 and DQ1 are valid bits and DQ<15:2> are don't care. Writes to address x0000 are not allowed from either port.

Address x0000 is not available for standard memory accesses when $\overline{SFEN}$ = V_{IL}. When $\overline{SFEN}$ = V_{IH}, address x0000 is available for memory accesses.

The inputs will be 1.8V/2.5V LVCMOS or 3.0V LVTTL, depending on the core voltage supply (V_{CC}). Refer to *Table 3* for Input Read Register operation.

IRR is not available in the CYDC256B16 and CYDC128B08, as the IRR pins are used as extra address pins A_{13L} and A_{13R}.

Output Drive Register

The Output Drive Register (ODR) determines the state of up to five external binary state devices by providing a path to V_{SS} for the external circuit. These outputs are Open Drain.

The five external devices can operate at different voltages ($1.5V \leq V_{DDIO} \leq 3.5V$) but the combined current cannot exceed 40 mA (8 mA max for each external device). The status of the ODR bits are set using standard write accesses from either port to address x0001 with a "1" corresponding to on and "0" corresponding to off.

The status of the ODR bits can be read with a standard read access to address x0001. When $\overline{SFEN}$ = V_{IL}, the ODR is active and address x0001 is not available for memory accesses. When $\overline{SFEN}$ = V_{IH}, the ODR is inactive and address x0001 can be used for standard accesses.

During reads and writes to ODR DQ<4:0> are valid and DQ<15:5> are don't care. Refer to *Table 4* for Output Drive Register operation.

Semaphore Operation

The CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available t_{SWRD} + t_{DOE} after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 5* shows sample semaphore operations.

When reading a semaphore, all sixteen/eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore. On power-up, both ports should write “1” to all eight semaphores.

Architecture

The CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 consist of an array of 4k, 8k, or 16k words of 16 dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). The CYDC064B08 and CYDC128B08 consist of an array of 8k and 16k words of 8 each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$).These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two Interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two Semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the devices can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The devices also have an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Table 1. Non-Contending Read/Write

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_8–I/O_{15}[11]	I/O_0–I/O_7	Operation
H	X	X	X	X	H	High Z	High Z	Deselected: Power-down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H	_⌐‾	X	X	X	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
X	_⌐‾	X	H	H	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Table 2. Interrupt Operation Example (Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH)[12]

Function	Left Port					Right Port				
	R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L-13L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R-13R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	3FFF[15]	X	X	X	X	X	L[14]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	3FFF[15]	H[13]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[13]	L	L	X	3FFE[15]	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	3FFE[15]	H[14]	X	X	X	X	X

Notes:
11. This column applies to x16 devices only.
12. See Interrupts Functional Description for specific highest memory locations by device.
13. If $\overline{BUSY}_R$ = L, then no change.
14. If $\overline{BUSY}_L$ = L, then no change.
15. See Functional Description for specific addresses by device.

Table 3. Input Read Register Operation[16, 19]

$\overline{SFEN}$	$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	ADDR	I/O_0–I/O_1	I/O_2–I/O_{15}	Mode
H	L	H	L	L	L	x0000-Max	VALID[17]	VALID[17]	Standard Memory Access
L	L	H	L	X	L	x0000	VALID[18]	X	IRR Read

Table 4. Output Drive Register [20]

$\overline{SFEN}$	$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	ADDR	I/O_0–I/O_4	I/O_5–I/O_{15}	Mode
H	L	H	X[21]	L[17]	L[17]	x0000-Max	VALID[17]	VALID[17]	Standard Memory Access
L	L	L	X	X	L	x0001	VALID[18]	X	ODR Write[20, 22]
L	L	H	L	X	L	x0001	VALID[18]	X	ODR Read[20]

Table 5. Semaphore Operation Example

Function	I/O_0–I/O_{15} Left	I/O_0–I/O_{15} Right	Status
No action	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free

Notes:
16. $\overline{SFEN}$ = V_{IL} for IRR reads.
17. $\overline{UB}$ or $\overline{LB}$ = V_{IL}. If $\overline{LB}$ = V_{IL}, then DQ<7:0> are valid. If $\overline{UB}$ = V_{IL} then DQ<15:8> are valid.
18. $\overline{LB}$ must be active ($\overline{LB}$ = V_{IL}) for these bits to be valid.
19. $\overline{SFEN}$ active when either $\overline{CE}_L$ = V_{IL} or $\overline{CE}_R$ = V_{IL}. It is inactive when $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}.
20. $\overline{SFEN}$ = V_{IL} for ODR reads and writes.
21. Output enable must be low ($\overline{OE}$ = V_{IL}) during reads for valid data to be output.
22. During ODR writes data will also be written to the memory.

Maximum Ratings[23]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with Power Applied..–55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +3.3V

DC Voltage Applied to Outputs in High-Z State..........................–0.5V to V_{CC} + 0.5V

DC Input Voltage[24] ....–0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)............................. 90 mA

Static Discharge Voltage... > 2000V

Latch-up Current.. > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	1.8V ± 100 mV 2.5V ± 100 mV 3.0V ± 300 mV
Industrial	–40°C to +85°C	1.8V ± 100 mV 2.5V ± 100 mV 3.0V ± 300 mV

Electrical Characteristics for V_{CC} = 1.8V Over the Operating Range

				CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08			CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08			
				-40			-55			
Parameter	Description	P1 I/O Voltage	P2 I/O Voltage	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage (I_{OH} = –100 µA)	1.8V (any port)		V_{DDIO} – 0.2			V_{DDIO} – 0.2			V
	Output HIGH Voltage (I_{OH} = –2 mA)	2.5V (any port)		2.0			2.0			V
	Output HIGH Voltage (I_{OH} = –2 mA)	3.0V (any port)		2.1			2.1			V
V_{OL}	Output LOW Voltage (I_{OL} = 100 µA)	1.8V (any port)				0.2			0.2	V
	Output HIGH Voltage (I_{OL} = 2 mA)	2.5V (any port)				0.4			0.4	V
	Output HIGH Voltage (I_{OL} = 2 mA)	3.0V (any port)				0.4			0.4	V
V_{OL} ODR	ODR Output LOW Voltage (I_{OL} = 8 mA)	1.8V (any port)				0.2			0.2	V
		2.5V (any port)				0.2			0.2	V
		3.0V (any port)				0.2			0.2	V
V_{IH}	Input HIGH Voltage	1.8V (any port)		1.2		V_{DDIO} + 0.2	1.2		V_{DDIO} + 0.2	V
		2.5V (any port)		1.7		V_{DDIO} + 0.3	1.7		V_{DDIO} + 0.3	V
		3.0V (any port)		2.0		V_{DDIO} + 0.2	2.0		V_{DDIO} + 0.2	V
V_{IL}	Input LOW Voltage	1.8V (any port)		–0.2		0.4	–0.2		0.4	V
		2.5V (any port)		–0.3		0.6	–0.3		0.6	V
		3.0V (any port)		–0.2		0.7	–0.2		0.7	V
I_{OZ}	Output Leakage Current	1.8V	1.8V	–1		1	–1		1	µA
		2.5V	2.5V	–1		1	–1		1	µA
		3.0V	3.0V	–1		1	–1		1	µA
I_{CEX} ODR	ODR Output Leakage Current. V_{OUT} = V_{DDIO}	1.8V	1.8V	–1		1	–1		1	µA
		2.5V	2.5V	–1		1	–1		1	µA
		3.0V	3.0V	–1		1	–1		1	µA

Notes:
23. The voltage on any input or I/O pin can not exceed the power pin during power-up.
24. Pulse width < 20 ns.

Electrical Characteristics for V_{CC} = 1.8V (continued) Over the Operating Range

					CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08			CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08			
					-40			-55			
Parameter	**Description**		**P1 I/O Voltage**	**P2 I/O Voltage**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{IX}	Input Leakage Current		1.8V	1.8V	–1		1	–1		1	µA
			2.5V	2.5V	–1		1	–1		1	µA
			3.0V	3.0V	–1		1	–1		1	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA) Outputs Disabled	Ind.	1.8V	1.8V		25	40		15	25	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$, $SEM_L = SEM_R = V_{CC} - 0.2$, $f = f_{MAX}$	Ind.	1.8V	1.8V		2	6		2	6	µA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$	Ind.	1.8V	1.8V		8.5	18		8.5	14	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC} - 0.2V$, SEM_L and $SEM_R > V_{CC} - 0.2V$, f = 0	Ind.	1.8V	1.8V		2	6		2	6	µA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$[25]	Ind.	1.8V	1.8V		8.5	18		8.5	14	mA

Notes:

25. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at $f = 1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Electrical Characteristics for V_{CC} = 2.5V Over the Operating Range

Parameter	Description		P1 I/O Voltage	P2 I/O Voltage	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40 Min.	Typ.	Max.	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage (I_{OH} = –2 mA)		2.5V (any port)		2.0			2.0			V
	Output HIGH Voltage (I_{OH} = –2 mA)		3.0V (any port)		2.1			2.1			V
V_{OL}	Output LOW Voltage (I_{OL} = 2 mA)		2.5V (any port)				0.4			0.4	V
	Output LOW Voltage (I_{OL} = 2 mA)		3.0V (any port)				0.4			0.4	V
V_{OL} ODR	ODR Output LOW Voltage (I_{OL} = 8 mA)		2.5V (any port)				0.2			0.2	V
			3.0V (any port)				0.2			0.2	V
V_{IH}	Input HIGH Voltage		2.5V (any port)		1.7		V_{DDIO} + 0.3	1.7		V_{DDIO} + 0.3	V
			3.0V (any port)		2.0		V_{DDIO} + 0.2	2.0		V_{DDIO} + 0.2	V
V_{IL}	Input LOW Voltage		2.5V (any port)		–0.3		0.6	–0.3		0.6	V
			3.0V (any port)		–0.2		0.7	–0.2		0.7	V
I_{OZ}	Output Leakage Current		2.5V	2.5V	–1		1	–1		1	µA
			3.0V	3.0V	–1		1	–1		1	µA
I_{CEX} ODR	ODR Output Leakage Current. $V_{OUT} = V_{CC}$		2.5V	2.5V	–1		1	–1		1	µA
			3.0V	3.0V	–1		1	–1		1	µA
I_{IX}	Input Leakage Current		2.5V	2.5V	–1		1	–1		1	µA
			3.0V	3.0V	–1		1	–1		1	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA) Outputs Disabled	Ind.	2.5V	2.5V		39	55		28	40	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$, $SEM_L = SEM_R = V_{CC} - 0.2$, $f = f_{MAX}$	Ind.	2.5V	2.5V		6	8		6	8	µA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$	Ind.	2.5V	2.5V		21	30		18	25	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC} - 0.2V$, SEM_L and $SEM_R > V_{CC} - 0.2V$, f = 0	Ind.	2.5V	2.5V		4	6		4	6	µA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$[25]	Ind.	2.5V	2.5V		21	30		18	25	mA

Electrical Characteristics for 3.0V Over the Operating Range

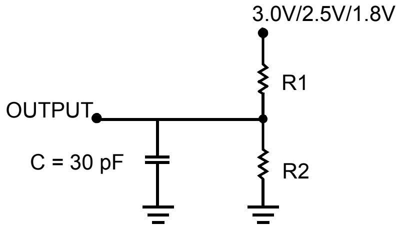
Parameter	Description		P1 I/O Voltage	P2 I/O Voltage	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40 Min.	-40 Typ.	-40 Max.	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55 Min.	-55 Typ.	-55 Max.	Unit
V_{OH}	Output HIGH Voltage (I_{OH} = –2 mA)		3.0V (any port)		2.1			2.1			V
V_{OL}	Output LOW Voltage (I_{OL} = 2 mA)		3.0V (any port)				0.4			0.4	V
V_{OL} ODR	ODR Output LOW Voltage (I_{OL} = 8 mA)		3.0V (any port)				0.2			0.2	V
V_{IH}	Input HIGH Voltage		3.0V (any port)		2.0		V_{DDIO} + 0.2	2.0		V_{DDIO} + 0.2	V
V_{IL}	Input LOW Voltage		3.0V (any port)		–0.2		0.7	–0.2		0.7	V
I_{OZ}	Output Leakage Current		3.0V	3.0V	–1		1	–1		1	µA
I_{CEX} ODR	ODR Output Leakage Current. $V_{OUT} = V_{CC}$		3.0V	3.0V	–1		1	–1		1	µA
I_{IX}	Input Leakage Current		3.0V	3.0V	–1		1	–1		1	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA) Outputs Disabled	Ind.	3.0V	3.0V		49	70		42	60	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$, $SEM_L = SEM_R = V_{CC} - 0.2$, $f = f_{MAX}$	Ind.	3.0V	3.0V		7	10		7	10	µA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$	Ind.	3.0V	3.0V		28	40		25	35	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC} - 0.2V$, SEM_L and $SEM_R > V_{CC} - 0.2V$, f = 0	Ind.	3.0V	3.0V		6	8		6	8	µA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$[25]	Ind.	3.0V	3.0V		28	40		25	35	mA

Capacitance[26]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V	9	pF
C_{OUT}	Output Capacitance		10	pF

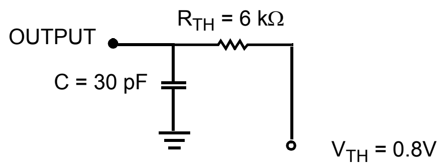
Note:
26. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



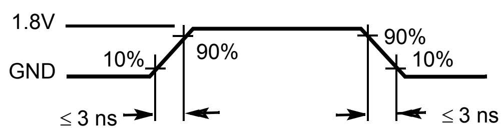
(a) Normal Load (Load 1)

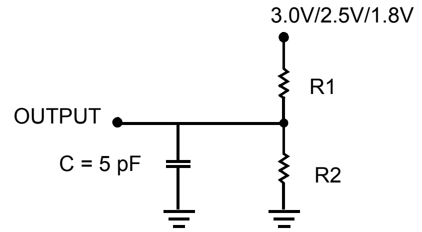
	3.0V/2.5V	1.8V
R1	1022Ω	13500Ω
R2	792Ω	10800Ω



(b) Thévenin Equivalent (Load 1)

ALL INPUT PULSES





(c) Three-State Delay (Load 2)

(Used for t_{LZ}, t_{HZ}, t_{HZWE}, and t_{LZWE} including scope and jig)

Switching Characteristics for V_{CC} = 1.8V Over the Operating Range[27]

Parameter	Description	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08		CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	40		55		ns
t_{AA}	Address to Data Valid		40		55	ns
t_{OHA}	Output Hold From Address Change	5		5		ns
t_{ACE}[28]	$\overline{CE}$ LOW to Data Valid		40		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30	ns
t_{LZOE}[29, 30, 31]	$\overline{OE}$ Low to Low Z	5		5		ns
t_{HZOE}[29, 30, 31]	$\overline{OE}$ HIGH to High Z		15		25	ns
t_{LZCE}[29, 30, 31]	$\overline{CE}$ LOW to Low Z	5		5		ns
t_{HZCE}[29, 30, 31]	$\overline{CE}$ HIGH to High Z		15		25	ns
t_{PU}[31]	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}[31]	$\overline{CE}$ HIGH to Power-Down		40		55	ns
t_{ABE}[28]	Byte Enable Access Time		40		55	ns
Write Cycle						
t_{WC}	Write Cycle Time	40		55		ns
t_{SCE}[28]	$\overline{CE}$ LOW to Write End	30		45		ns
t_{AW}	Address Valid to Write End	30		45		ns

Notes:
27. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC}, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
28. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
29. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
30. Test conditions used are Load 3.
31. This parameter is guaranteed but not tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform

Switching Characteristics for V_{CC} = 1.8V Over the Operating Range[27] (continued)

Parameter	Description	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08		CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
t_{HA}	Address Hold From Write End	0		0		ns
t_{SA}[28]	Address Set-up to Write Start	0		0		ns
t_{PWE}	Write Pulse Width	25		40		ns
t_{SD}	Data Set-up to Write End	20		30		ns
t_{HD}	Data Hold From Write End	0		0		ns
t_{HZWE}[30, 31]	R/$\overline{W}$ LOW to High Z		15		25	ns
t_{LZWE}[30, 31]	R/$\overline{W}$ HIGH to Low Z	0		0		ns
t_{WDD}[32]	Write Pulse to Data Delay		55		80	ns
t_{DDD}[32]	Write Data Valid to Read Data Valid		55		80	ns
Busy Timing[33]						
t_{BLA}	$\overline{\text{BUSY}}$ LOW from Address Match		30		45	ns
t_{BHA}	$\overline{\text{BUSY}}$ HIGH from Address Mismatch		30		45	ns
t_{BLC}	$\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW		30		45	ns
t_{BHC}	$\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH		30		45	ns
t_{PS}[34]	Port Set-up for Priority	5		5		ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{\text{BUSY}}$ (Slave)	0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{\text{BUSY}}$ HIGH (Slave)	20		35		ns
t_{BDD}[35]	$\overline{\text{BUSY}}$ HIGH to Data Valid		30		40	ns
Interrupt Timing[33]						
t_{INS}	$\overline{\text{INT}}$ Set Time		35		45	ns
t_{INR}	$\overline{\text{INT}}$ Reset Time		35		45	ns
Semaphore Timing						
t_{SOP}	SEM Flag Update Pulse ($\overline{\text{OE}}$ or $\overline{\text{SEM}}$)	10		15		ns
t_{SWRD}	SEM Flag Write to Read Time	10		10		ns
t_{SPS}	SEM Flag Contention Window	10		10		ns
t_{SAA}	SEM Address Access Time		40		55	ns

Notes:
32. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
33. Test conditions used are Load 2.
34. Add 2ns to this value when the I/O ports are operating at different voltages.
35. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{DDD}–t_{SD} (actual).

Switching Characteristics for V_{CC} = 2.5V Over the Operating Range

Parameter	Description	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40		CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	40		55		ns
t_{AA}	Address to Data Valid		40		55	ns
t_{OHA}	Output Hold From Address Change	5		5		ns
t_{ACE}[28]	$\overline{CE}$ LOW to Data Valid		40		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30	ns
t_{LZOE}[29, 30, 31]	$\overline{OE}$ Low to Low Z	2		2		ns
t_{HZOE}[29, 30, 31]	$\overline{OE}$ HIGH to High Z		15		15	ns
t_{LZCE}[29, 30, 31]	$\overline{CE}$ LOW to Low Z	2		2		ns
t_{HZCE}[29, 30, 31]	$\overline{CE}$ HIGH to High Z		15		15	ns
t_{PU}[31]	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}[31]	$\overline{CE}$ HIGH to Power-Down		40		55	ns
t_{ABE}[28]	Byte Enable Access Time		40		55	ns
Write Cycle						
t_{WC}	Write Cycle Time	40		55		ns
t_{SCE}[28]	$\overline{CE}$ LOW to Write End	30		45		ns
t_{AW}	Address Valid to Write End	30		45		ns
t_{HA}	Address Hold From Write End	0		0		ns
t_{SA}[28]	Address Set-up to Write Start	0		0		ns
t_{PWE}	Write Pulse Width	25		40		ns
t_{SD}	Data Set-up to Write End	20		30		ns
t_{HD}	Data Hold From Write End	0		0		ns
t_{HZWE}[30, 31]	R/$\overline{W}$ LOW to High Z		15		25	ns
t_{LZWE}[30, 31]	R/$\overline{W}$ HIGH to Low Z	0		0		ns
t_{WDD}[32]	Write Pulse to Data Delay		55		80	ns
t_{DDD}[32]	Write Data Valid to Read Data Valid		55		80	ns
Busy Timing[33]						
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		30		45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		30		45	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		30		45	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		30		45	ns
t_{PS}[34]	Port Set-up for Priority	5		5		ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	20		35		ns
t_{BDD}[35]	$\overline{BUSY}$ HIGH to Data Valid		30		40	ns

Switching Characteristics for V_{CC} = 2.5V Over the Operating Range (continued)

Parameter	Description	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40		CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55		Unit
		Min.	Max.	Min.	Max.	
Interrupt Timing[33]						
t_{INS}	$\overline{INT}$ Set Time		35		45	ns
t_{INR}	$\overline{INT}$ Reset Time		35		45	ns
Semaphore Timing						
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		15		ns
t_{SWRD}	SEM Flag Write to Read Time	10		10		ns
t_{SPS}	SEM Flag Contention Window	10		10		ns
t_{SAA}	SEM Address Access Time		40		55	ns

Switching Characteristics for V_{CC} = 3.0V Over the Operating Range

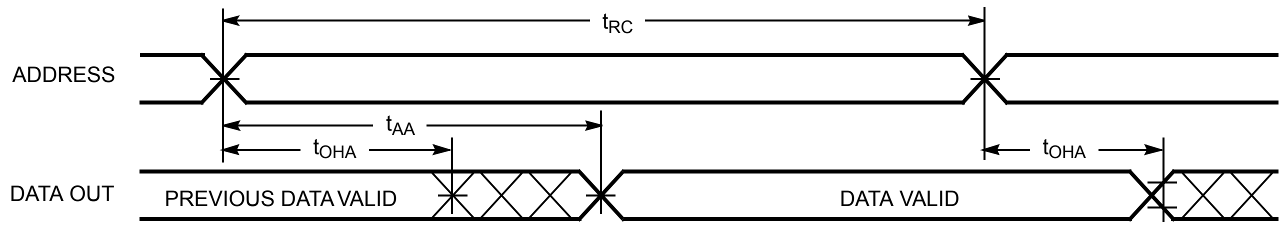
Parameter	Description	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40		CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	40		55		ns
t_{AA}	Address to Data Valid		40		55	ns
t_{OHA}	Output Hold From Address Change	5		5		ns
t_{ACE}[28]	$\overline{CE}$ LOW to Data Valid		40		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30	ns
t_{LZOE}[29, 30, 31]	$\overline{OE}$ Low to Low Z	1		1		ns
t_{HZOE}[29, 30, 31]	$\overline{OE}$ HIGH to High Z		15		15	ns
t_{LZCE}[29, 30, 31]	$\overline{CE}$ LOW to Low Z	1		1		ns
t_{HZCE}[29, 30, 31]	$\overline{CE}$ HIGH to High Z		15		15	ns
t_{PU}[31]	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}[31]	$\overline{CE}$ HIGH to Power-Down		40		55	ns
t_{ABE}[28]	Byte Enable Access Time		40		55	ns
Write Cycle						
t_{WC}	Write Cycle Time	40		55		ns
t_{SCE}[28]	$\overline{CE}$ LOW to Write End	30		45		ns
t_{AW}	Address Valid to Write End	30		45		ns
t_{HA}	Address Hold From Write End	0		0		ns
t_{SA}[28]	Address Set-up to Write Start	0		0		ns
t_{PWE}	Write Pulse Width	25		40		ns
t_{SD}	Data Set-up to Write End	20		30		ns
t_{HD}	Data Hold From Write End	0		0		ns

Switching Characteristics for V_{CC} = 3.0V Over the Operating Range (continued)

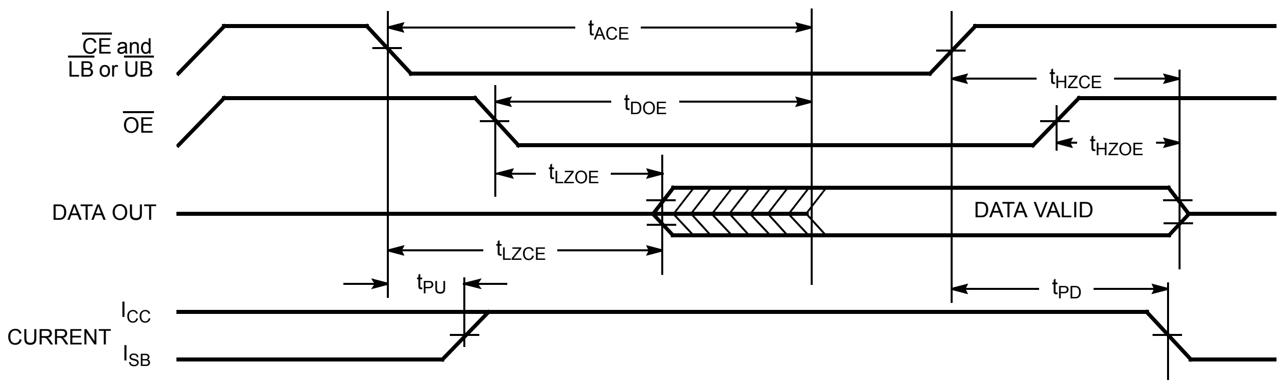
Parameter	Description	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -40		CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08 -55		Unit
		Min.	Max.	Min.	Max.	
t_{HZWE}[30, 31]	R/$\overline{W}$ LOW to High Z		15		25	ns
t_{LZWE}[30, 31]	R/$\overline{W}$ HIGH to Low Z	0		0		ns
t_{WDD}[32]	Write Pulse to Data Delay		55		80	ns
t_{DDD}[32]	Write Data Valid to Read Data Valid		55		80	ns
Busy Timing[33]						
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		30		45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		30		45	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		30		45	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		30		45	ns
t_{PS}[34]	Port Set-up for Priority	5		5		ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	20		35		ns
t_{BDD}[35]	$\overline{BUSY}$ HIGH to Data Valid		30		40	ns
Interrupt Timing[33]						
t_{INS}	$\overline{INT}$ Set Time		35		45	ns
t_{INR}	$\overline{INT}$ Reset Time		35		45	ns
Semaphore Timing						
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		15		ns
t_{SWRD}	SEM Flag Write to Read Time	10		10		ns
t_{SPS}	SEM Flag Contention Window	10		10		ns
t_{SAA}	SEM Address Access Time		40		55	ns

Switching Waveforms

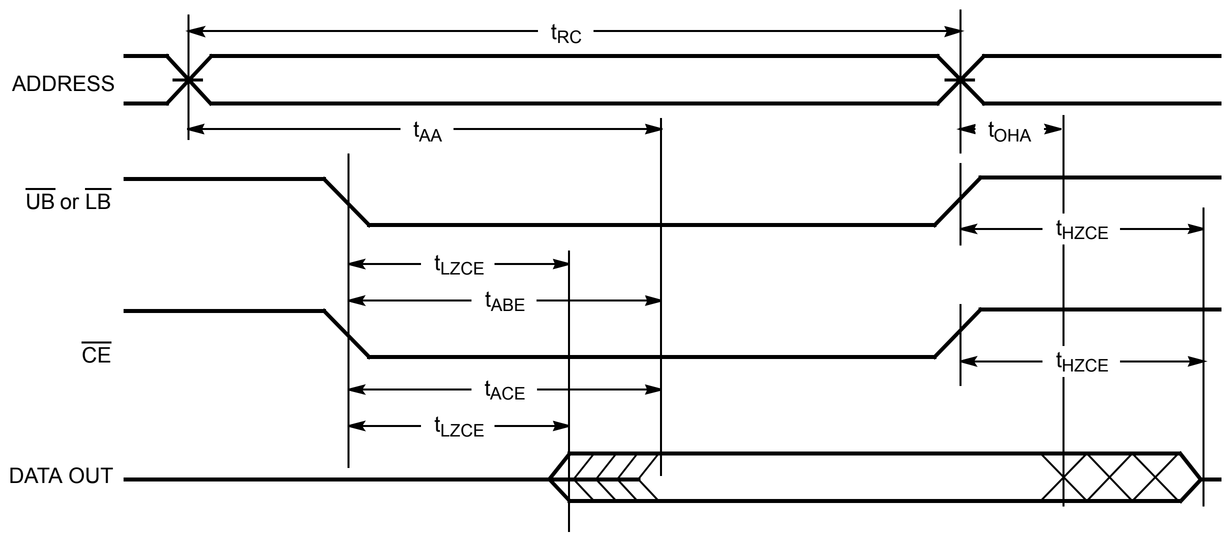
Read Cycle No.1 (Either Port Address Access)[36, 37, 38]



Read Cycle No.2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[36, 39, 40]



Read Cycle No. 3 (Either Port)[36, 38, 41, 42]

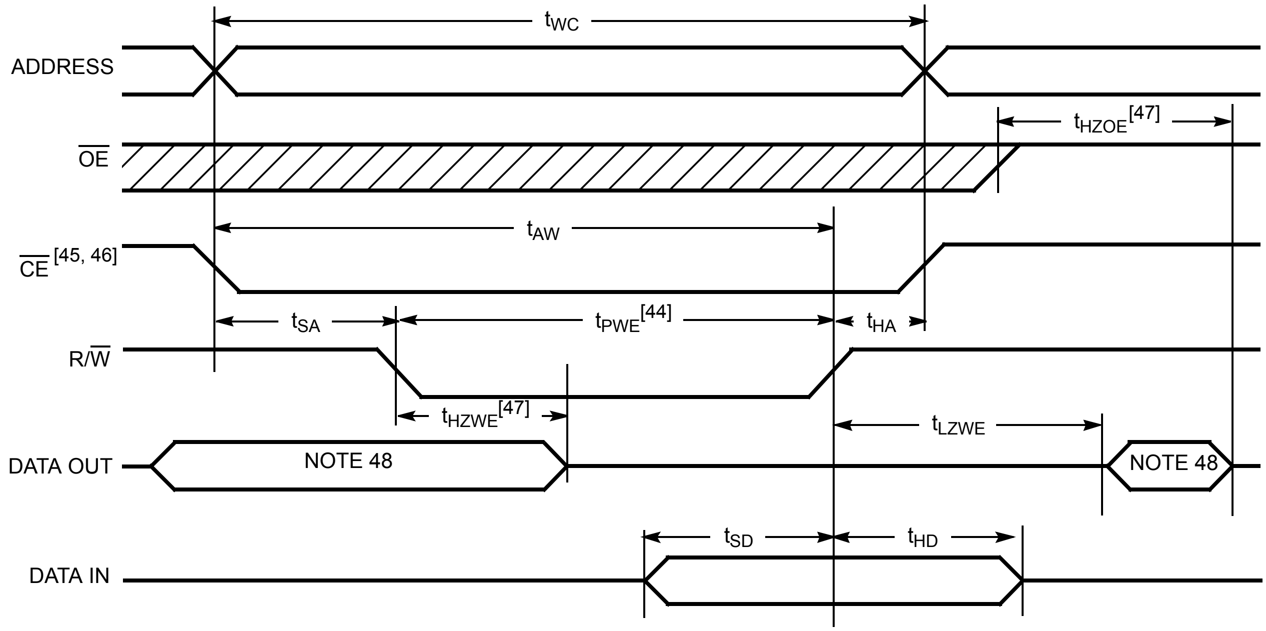


Notes:

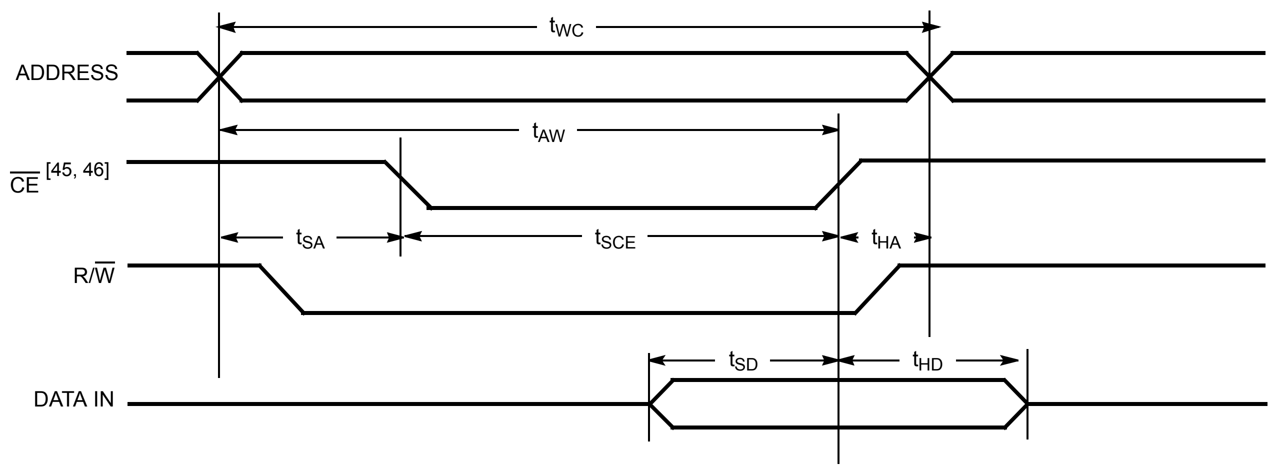
36. R/$\overline{W}$ is HIGH for read cycles.
37. Device is continuously selected $\overline{CE}$ = V_{IL} and $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
38. $\overline{OE}$ = V_{IL}.
39. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
40. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.
41. R/$\overline{W}$ must be HIGH during all address transitions.
42. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.

Switching Waveforms (continued)

Write Cycle No.1: R/W Controlled Timing[41, 42, 43, 44, 45, 46]



Write Cycle No. 2: CE Controlled Timing[41, 42, 43, 48]

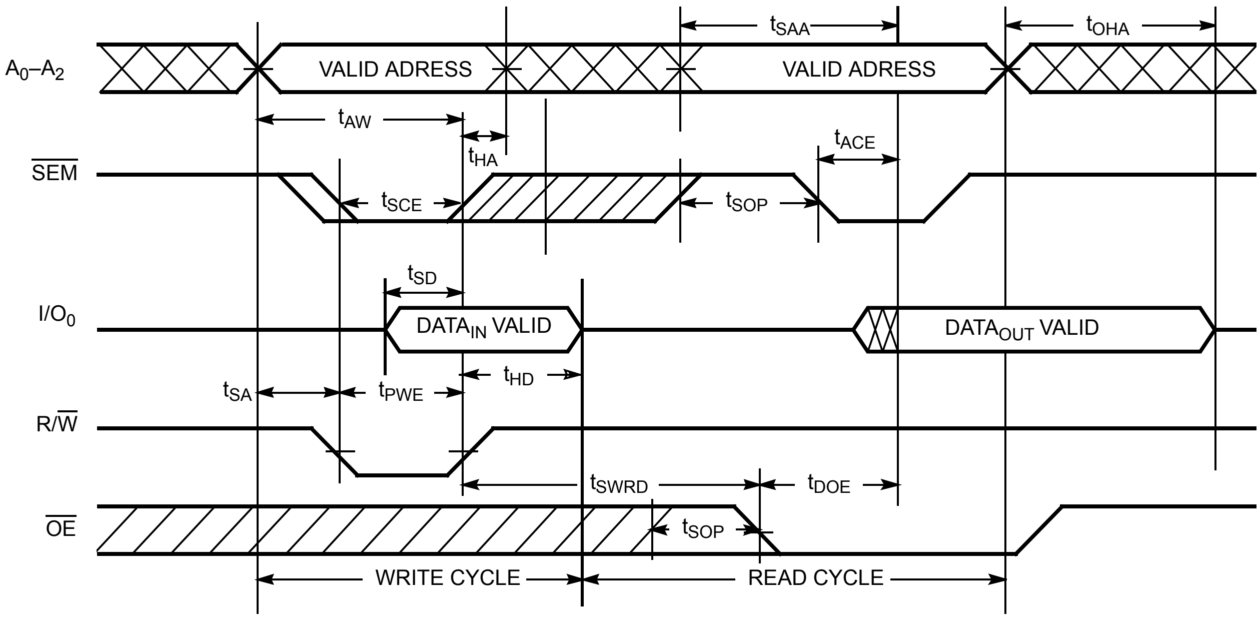


Notes:

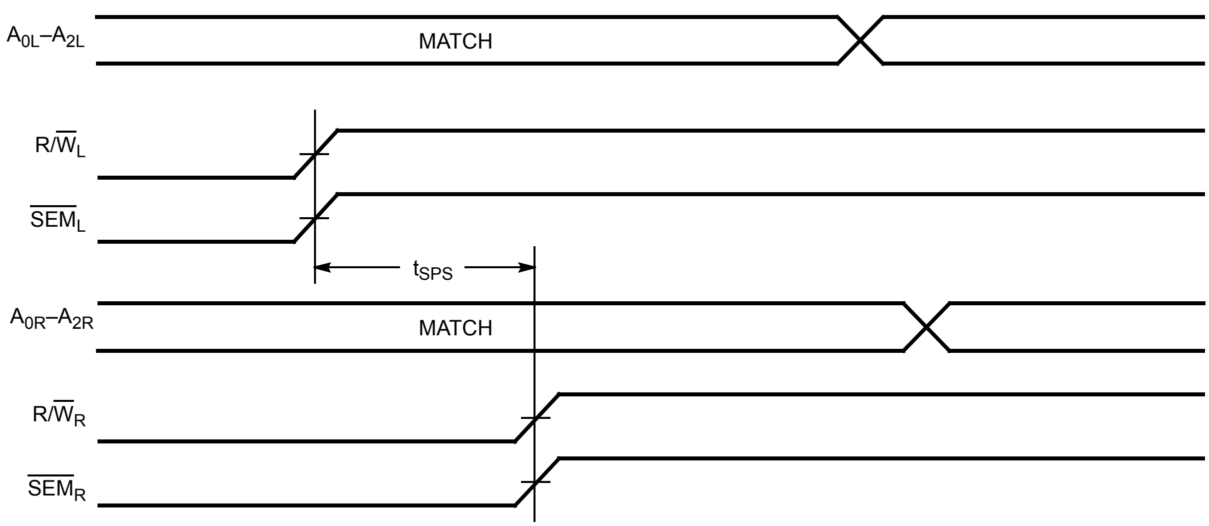
43. t_{HA} is measured from the earlier of CE or R/W or (SEM or R/W) going HIGH at the end of write cycle.
44. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
45. To access RAM, CE = V_{IL}, SEM = V_{IH}.
46. To access upper byte, CE = V_{IL}, UB = V_{IL}, SEM = V_{IH}.
    To access lower byte, CE = V_{IL}, LB = V_{IL}, SEM = V_{IH}.
47. Transition is measured ±0 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
48. During this period, the I/O pins are in the output state, and input signals must not be applied.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[49, 50]



Timing Diagram of Semaphore Contention[51, 52]

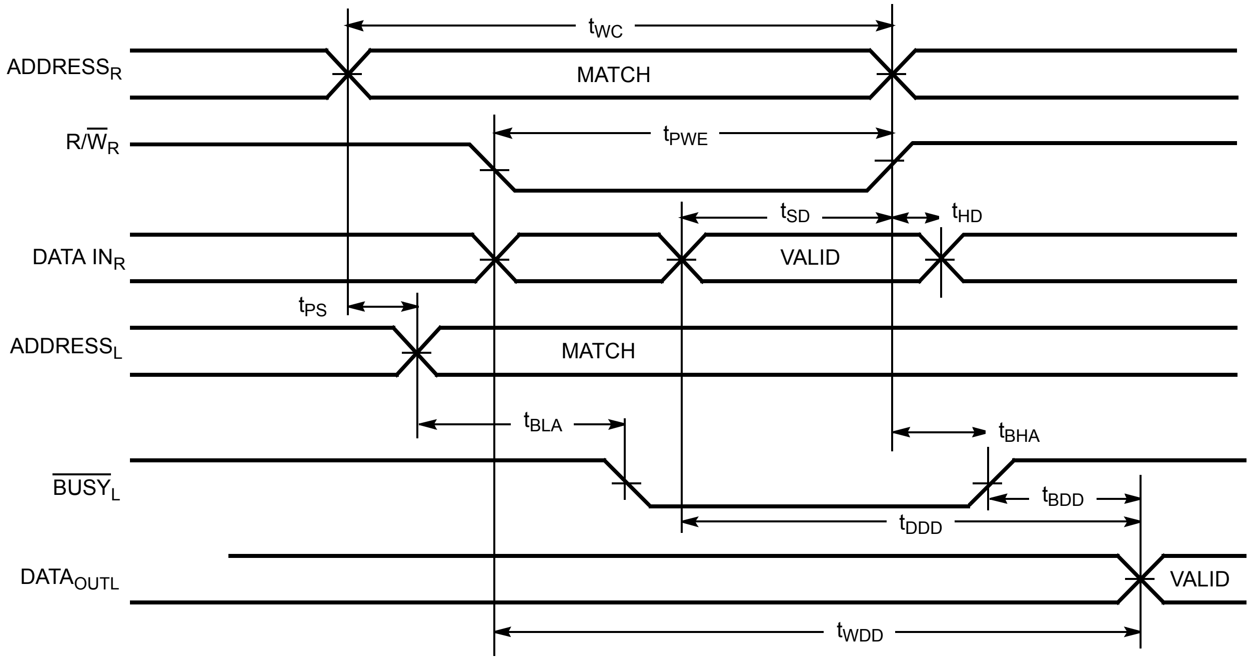


Notes:

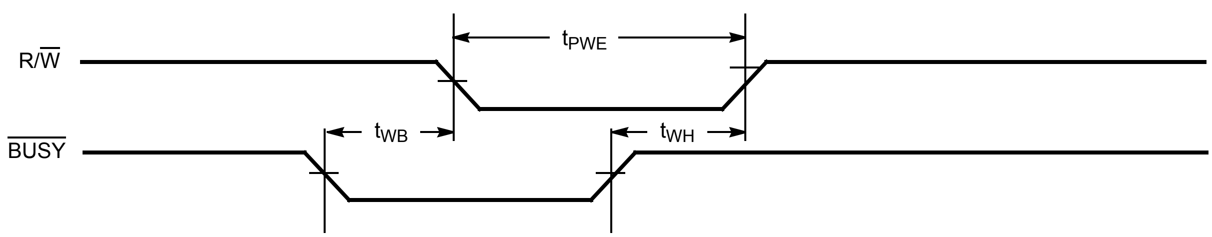
49. If the CE or SEM LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.
50. CE = HIGH for the duration of the above timing (both write and read cycle).
51. I/O_{0R} = I/O_{0L} = LOW (request semaphore); $\overline{CE}_R$ = $\overline{CE}_L$ = HIGH.
52. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Timing Diagram of Read with BUSY (M/S=HIGH)[53]



Write Timing with Busy Input (M/S = LOW)

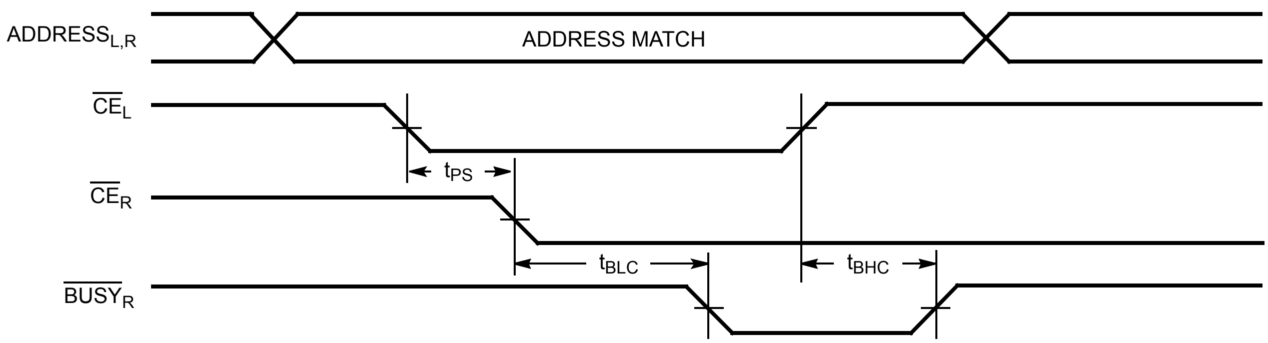


Note:
53. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

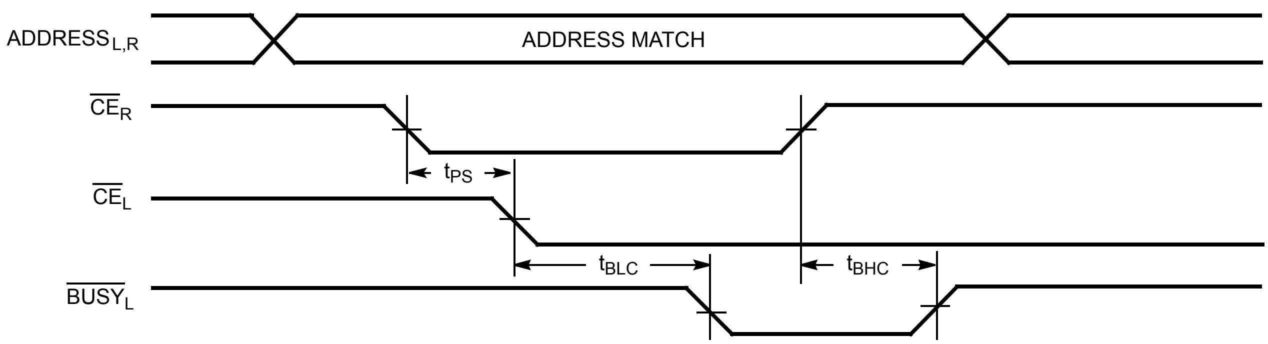
Switching Waveforms (continued)

Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First[54]

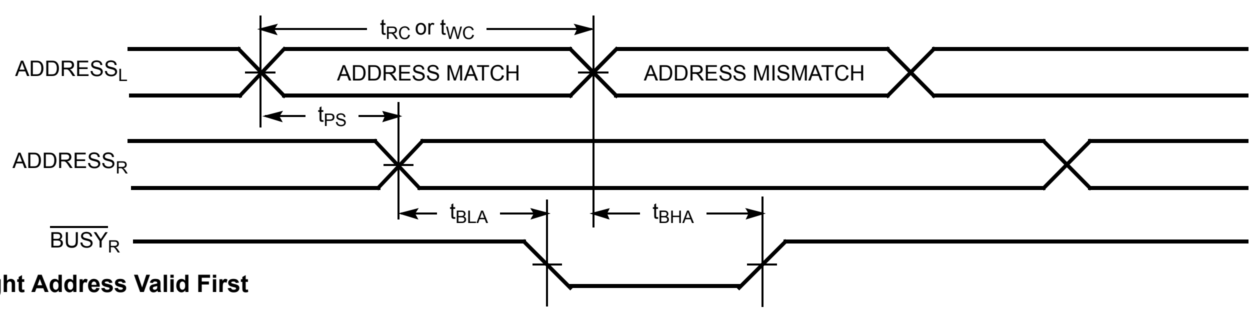


$\overline{CE}_R$ Valid First

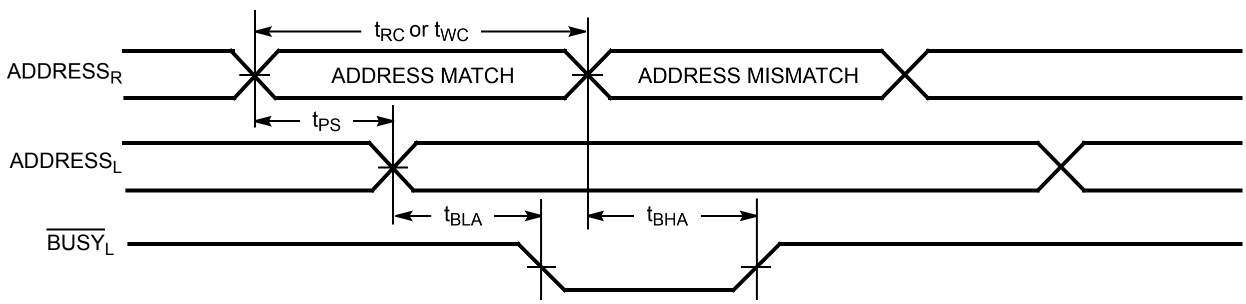


Busy Timing Diagram No.2 (Address Arbitration)[54]

Left Address Valid First



Right Address Valid First



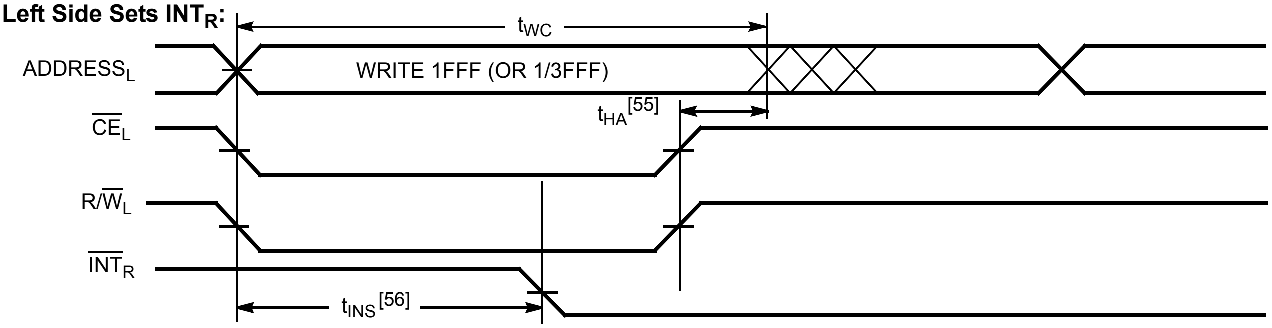
Note:

54. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

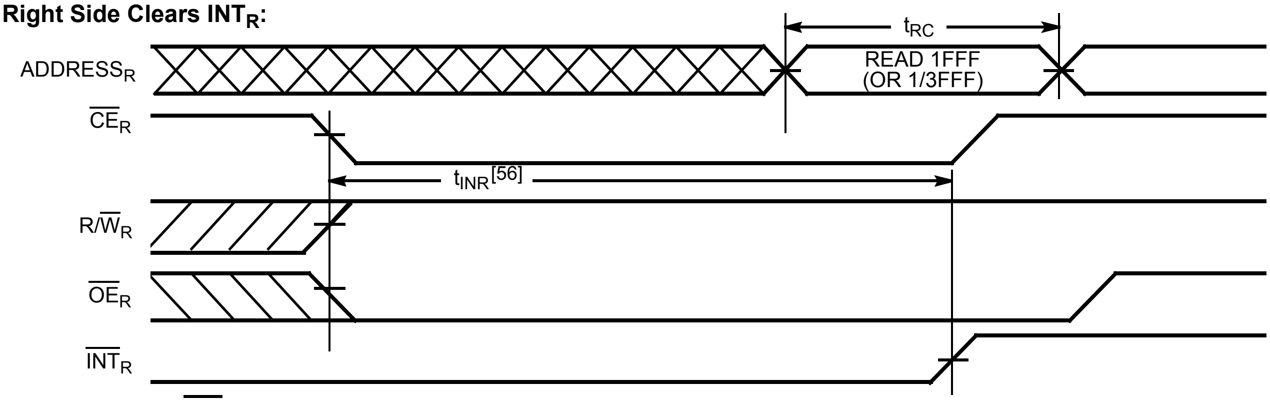
Switching Waveforms (continued)

Interrupt Timing Diagrams

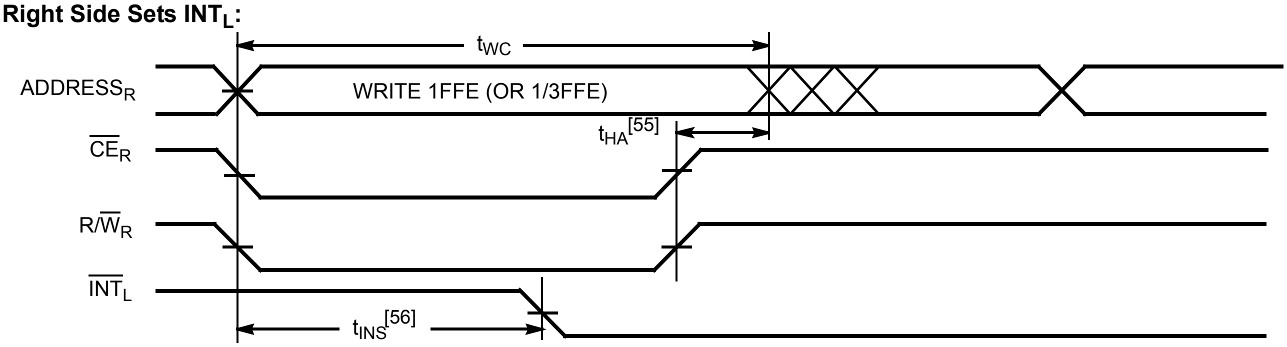
Left Side Sets $\overline{INT}_R$:



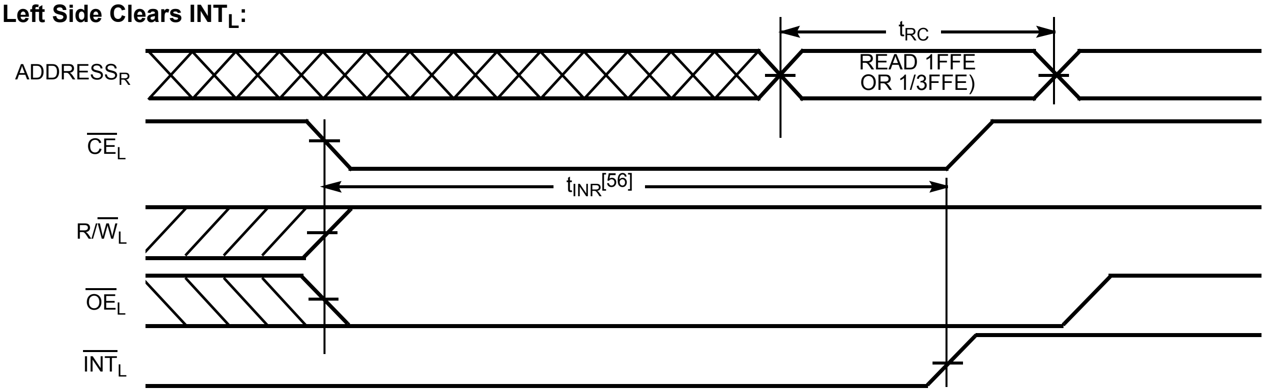
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Notes:
55. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
56. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Ordering Information

16k x16 1.8V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDC256B16-40AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC256B16-55AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC256B16-55AXI	AZ0AB	100-pin Lead-free TQFP	Industrial

8k x16 1.8V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDC128B16-40AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC128B16-55AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC128B16-55AXI	AZ0AB	100-pin Lead-free TQFP	Industrial

4k x16 1.8V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDC064B16-40AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC064B16-55AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC064B16-55AXI	AZ0AB	100-pin Lead-free TQFP	Industrial

16k x8 1.8V Asynchronous Dual-Port SRAM

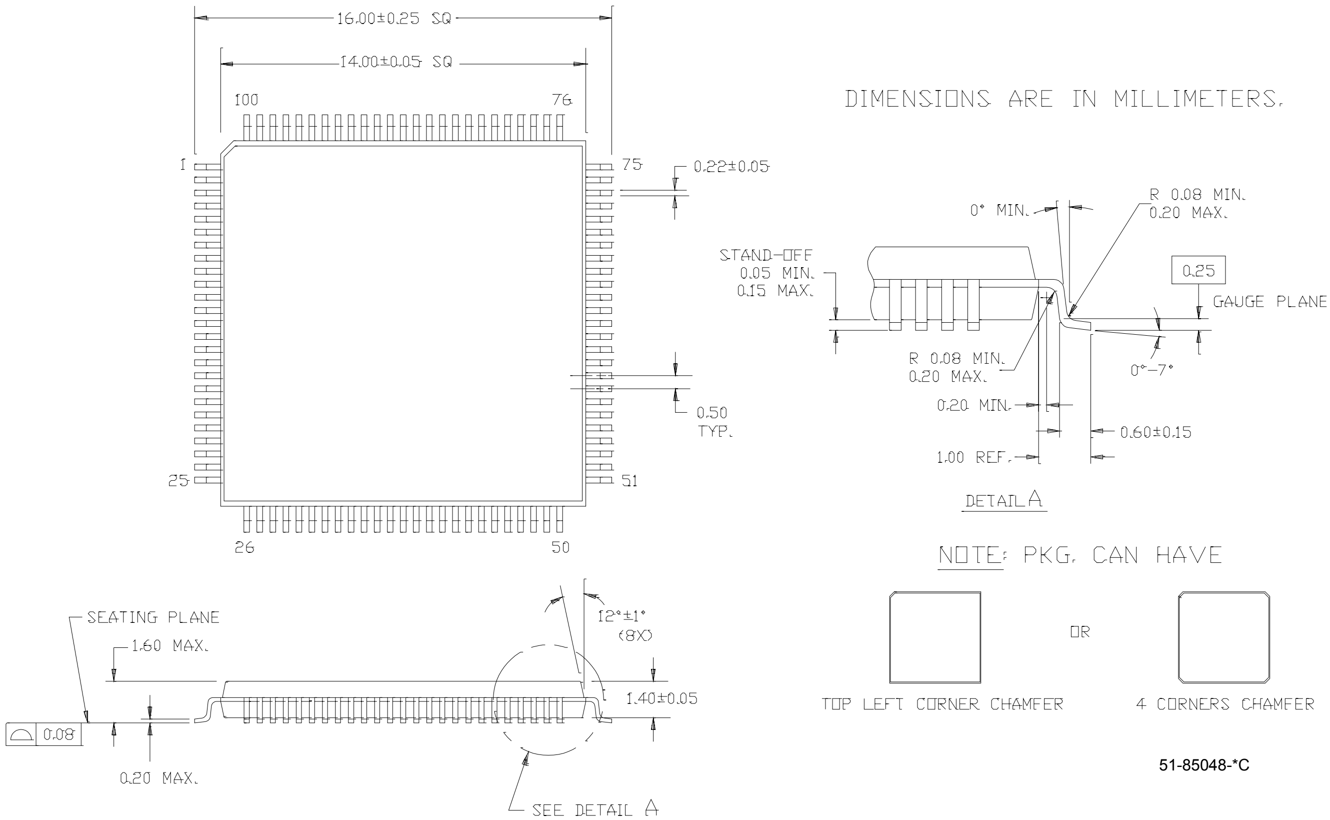
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDC128B08-40AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC128B08-55AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC128B08-55AXI	AZ0AB	100-pin Lead-free TQFP	Industrial

8k x8 1.8V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDC064B08-40AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC064B08-55AXC	AZ0AB	100-pin Lead-free TQFP	Commercial
55	CYDC064B08-55AXI	AZ0AB	100-pin Lead-free TQFP	Industrial

Package Diagram

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



51-85048-*C

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Document History Page

Document Title: CYDC256B16/CYDC128B16/CYDC064B16/CYDC128B08/CYDC064B08 1.8V 4k/8k/16k x 16 and 8k/16k x 8 ConsuMoBL Dual-Port Static RAM Document Number: 001-01638				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	385185	SEE ECN	YDT	New data sheet
*A	396697	SEE ECN	KGH	Updated ISB2 and ISB4 typo to mA. Updated tINS and tINR for -55 to 31ns.
*B	404777	SEE ECN	KGH	Updated I_{OH} and I_{OL} values for the 1.8V, 2.5V and 3.0V parameters V_{OH} and V_{OL} Replaced -35 speed bin with -40 Updated Switching Characteristics for V_{CC} = 2.5V and V_{CC} = 3.0V Included note 34
*C	463014	SEE ECN	HKH	Changed spec title to from “Consumer Dual-Port” to “ConsuMoBL Dual-Port” Cypress Internet Release
*D	505803	SEE ECN	HKH	Corrected typo in Features and Ordering Info sections. Cypress external web release.
*E	735537	SEE ECN	HKH	Corrected typo in Pg5 power supply section Updated tDDD timing value to be consistent with tWDD